

Table of Contents

Preface

1 Introduction

1.1 Organization	1-1
1.2 Requirements Terminology	1-2
1.3 Requirement Labeling Conventions	1-3
1.3.1 Numbering of Requirement Objects	1-3
1.3.2 Identification of Object Content	1-4
1.4 Change History	1-4
1.4.1 Changes from Issue 3 to Issue 4	1-4
1.4.2 Changes Between Issue 2 and Issue 3	1-5
1.4.3 Changes Between Issue 1 and Issue 2	1-7
1.4.4 Requirement Object Absolute Number Assignment	1-8

2 Availability

2.1 Introduction and Scope	2-1
2.1.1 Definition of Availability	2-1
2.1.2 Channel Outage Definition	2-1
2.1.3 Short-Haul Objective	2-2
2.1.4 Factors Contributing to Channel Unavailability	2-2
2.2 Interoffice Transport Systems	2-2
2.2.1 Asynchronous Transport Systems	2-3
2.2.1.1 DS3 Channel Availability Objectives	2-5
2.2.1.2 Hardware Allocation	2-6
2.2.1.3 Systems That Interface Directly at the DS1 or Other Sub-DS3 Level	2-7
2.2.1.4 Single Protection Switching Section HRCs	2-8
2.2.2 SONET Terminal Multiplexers	2-9
2.2.2.1 Unavailability Requirements and Objectives for a 250-Mile Route	2-9
2.2.2.2 Unavailability Requirements and Objectives for a 50-Mile Route	2-11
2.2.3 SONET ADMs	2-13
2.3 Loop Transport Networks	2-14
2.3.1 Subscriber Line Availability	2-14
2.3.2 HRC	2-14
2.3.2.1 Metallic Loop Reference Circuit	2-15
2.3.2.2 Fiber Optic Loop Reference Circuit	2-16
2.4 Loop Feeder Transport Systems	2-17
2.4.1 Asynchronous Transmission	2-18
2.4.2 SONET Transport	2-19

3 Reliability and Quality

3.1 System Reliability Objectives	3-1
3.1.1 Customer Service	3-1
3.1.2 Maintenance	3-2
3.1.3 Silent Failures	3-2
3.1.4 Interface to Operations Systems	3-2

- 3.1.5 Infant Mortality 3-2
- 3.2 Equipment Reliability Prediction 3-3
 - 3.2.1 Electronic Equipment 3-3
 - 3.2.2 Electromechanical Equipment 3-4
 - 3.2.3 System Reliability Modeling 3-4
- 3.3 Device Reliability 3-6
- 3.4 Manufacturing Program 3-7
- 3.5 Software Reliability and Quality 3-7
- 3.6 Customer's Reliability and Quality Surveillance Program 3-8
- 3.7 Customer's Field Performance Study 3-9

4 Error Performance

- 4.1 Scope of the Criteria 4-1
- 4.2 Error Performance Parameters 4-2
- 4.3 Error Performance Requirements 4-2

5 Protection Switching

- 5.1 Introduction 5-1
- 5.2 Protection Switching for Digital Radio Systems 5-2
 - 5.2.1 Architecture 5-2
 - 5.2.2 Switch Initiation Criteria 5-2
 - 5.2.3 Detection Time 5-2
 - 5.2.4 Switch Completion Time and Error Performance During Switching 5-3
 - 5.2.5 Restoration 5-3
- 5.3 Protection Switching for Fiber Optic Systems 5-3
 - 5.3.1 Architecture 5-4
 - 5.3.2 Switch Initiation 5-4
 - 5.3.2.1 Switch Initiation Thresholds 5-4
 - 5.3.2.2 Unwanted Switch Initiations 5-4
 - 5.3.3 Detection Time 5-5
 - 5.3.4 Switch Completion Time 5-6
 - 5.3.5 Restoration 5-7
- 5.4 Protection Switch Availability and Reliability 5-8
 - 5.4.1 Silent Failures 5-8
 - 5.4.2 Exercising 5-8
 - 5.4.3 Silent Failure Outages 5-9
 - 5.4.4 Exerciser Operation 5-9
- 5.5 Supplier-Provided Information and Monitoring Capabilities 5-10
 - 5.5.1 Fiber Optic Systems 5-10
 - 5.5.2 Radio Systems 5-11
- 5.6 Protection Switching for Terminal Circuit Packs 5-11
 - 5.6.1 Failure Detection, Switch Completion, and Error Performance During Switching 5-11
 - 5.6.2 Restoration 5-13

6 System Transient Response

- 6.1 Phase Hits 6-1
- 6.2 Temporary Signal Interruption 6-2
 - 6.2.1 Fiber Optic Systems 6-2

6.2.2 Radio Systems	6-2
6.3 Loss of Signal	6-2
7 Jitter	
7.1 Introduction	7-1
7.2 Network Interface Timing Jitter	7-2
7.3 Digital Equipment Timing Jitter	7-3
7.3.1 Jitter Tolerance	7-4
7.3.2 Jitter Transfer	7-7
7.3.3 Jitter Generation	7-13
7.3.4 Jitter Enhancement	7-14
8 Transmission Delay	
8.1 Background	8-1
8.2 Requirements	8-1
9 Signal Interfaces	
9.1 Line Codes and Pulse Density Assurance	9-1
9.1.1 BNZS/HDBN Coding	9-2
9.1.1.1 Bipolar with 8 Zero Substitution (B8ZS)	9-2
9.1.1.2 Bipolar with 6 Zero Substitution (B6ZS)	9-3
9.1.1.3 High Density Bipolar of Order 3 (HDB3)	9-3
9.1.1.4 Bipolar with 3 Zero Substitution (B3ZS)	9-3
9.1.2 Zero Code Suppression	9-4
9.1.3 Coded Mark Inversion	9-4
9.2 Synchronous Digital Data Interface - 64 kb/s and Lower	9-5
9.2.1 Connectors	9-5
9.2.2 Electrical Specifications	9-7
9.2.2.1 Transverse Balance	9-7
9.2.2.2 Isolation from Ground	9-10
9.2.2.3 Simplex Path	9-10
9.2.3 Transmitted Signal	9-10
9.2.3.1 Line Rates	9-11
9.2.3.2 Timing Accuracy	9-12
9.2.3.3 Isochronous and Peak Individual Distortion (Jitter)	9-12
9.2.3.4 Line Code	9-13
9.2.3.5 Pulse Amplitude	9-13
9.2.3.6 Transmit Filter	9-14
9.2.3.7 Frequency Domain Bound	9-14
9.2.3.8 Line Coupling	9-15
9.2.4 Received Signal	9-15
9.3 DS1 Interface	9-17
9.4 DS1C Interface	9-21
9.5 DS2 Interface	9-24
9.6 DS3 Interface	9-26
9.7 DS4NA Interface	9-30
9.8 Digital Hierarchy Interworking Interfaces - DS1A	9-34

10 Signal Formats

10.1 Synchronous Digital Data	10-1
10.1.1 Signal Format for Synchronous Digital Data without Secondary Channel	10-1
10.1.1.1 2.4- to 56-kb/s Data Rates	10-1
10.1.1.1.1 Frame Structure	10-1
10.1.1.1.2 Coding and Decoding Rules	10-1
10.1.1.1.3 Control Signals	10-2
10.1.1.1.3.A Normal Operation	10-2
10.1.1.1.3.B Maintenance	10-2
10.1.1.2 64-kb/s Data Rate	10-3
10.1.1.2.1 Frame Structure	10-3
10.1.1.2.2 Coding Restrictions	10-4
10.1.1.2.3 Idle Code	10-4
10.1.1.2.4 Control Signals	10-4
10.1.2 Signal Format for Synchronous Digital Data with Secondary Channel	10-5
10.1.2.1 Frame Structure	10-6
10.1.2.2 Coding and Decoding Rules	10-6
10.1.2.2.1 Primary Channel	10-6
10.1.2.2.2 Secondary Channel	10-7
10.1.2.3 Idle Code	10-8
10.1.2.4 Maintenance and Failure Signals	10-9
10.2 DS0	10-11
10.2.1 Voice	10-11
10.2.2 Synchronous Digital Data	10-11
10.2.2.1 DS0-A Mappings	10-12
10.2.2.1.1 2.4-, 4.8-, and 9.6-kb/s Rate DS0-A Mappings	10-12
10.2.2.1.2 19.2-kb/s Rate DS0-A Mapping	10-13
10.2.2.1.3 56-kb/s Rate DS0-A Mapping	10-13
10.2.2.1.4 64-kb/s Rate DS0-A Mapping	10-13
10.2.2.2 DS0-B Mappings	10-14
10.2.2.2.1 2.4-, 4.8-, and 9.6-kb/s Rate DS0-B Mappings	10-14
10.2.2.2.2 19.2-kb/s Rate DS0-B Mapping	10-15
10.2.2.3 Error Correction	10-15
10.2.2.3.1 DS0-A Error Correction	10-16
10.2.2.3.1.A DS0-A Error Correction at the 2.4-, 4.8-, and 9.6-kb/s Rates	10-16
10.2.2.3.1.B DS0-A Error Correction at the 19.2-kb/s Rate	10-16
10.2.2.3.1.C DS0-A Error Correction at the 56- and 64-kb/s Rates	10-17
10.2.2.3.2 Error Correction for the DS0-B	10-17
10.2.2.4 Maintenance and Control Functions	10-17
10.2.2.4.1 Control Codes	10-18
10.2.2.4.2 Loopback Activation	10-19
10.2.2.4.2.A Non-Latching Loopback	10-19
10.2.2.4.2.B Latching Loopback	10-20
10.3 DS1	10-24
10.3.1 Multiframe Arrangements: Superframe	10-24
10.3.1.1 Framing	10-24
10.3.1.2 Superframe Alarm Handling	10-25
10.3.2 Multiframe Arrangements: Extended Superframe	10-26

10.3.2.1 Framing	10-26
10.3.2.2 Cyclic Redundancy Check	10-28
10.3.2.3 ESF Data Link	10-28
10.3.2.3.1 Idle Code	10-28
10.3.2.3.2 Scheduled Performance Report Message	10-29
10.3.2.3.2.A Transmission Error Events	10-29
10.3.2.3.2.B Scheduled Performance Report Message Format	10-30
10.3.2.3.3 Unscheduled Messages	10-36
10.3.2.3.3.A Unscheduled Message Format	10-36
10.3.2.3.3.B Priority Messages	10-36
10.3.2.3.3.C Command and Response Messages	10-37
10.3.2.3.4 ESF Interworking	10-40
10.3.3 Alarm and Idle Signals	10-40
10.3.3.1 Alarm Indication Signal	10-40
10.3.3.2 DS1 Idle Code	10-40
10.3.3.3 DS1 RAI	10-41
10.3.4 Applications	10-41
10.3.4.1 Unchannelized	10-41
10.3.4.2 Channelized - 24 Channels	10-41
10.3.4.2.1 Robbed-Bit Signaling	10-41
10.3.4.2.2 64 kb/s Clear Channel Capability	10-42
10.3.4.2.3 Synchronous Digital Data	10-42
10.3.4.3 ISDN Primary Rate Access	10-42
10.3.4.4 Channelized - Other	10-42
10.4 DS1C	10-43
10.4.1 DS1C Frame Structure	10-43
10.4.2 Alarm Signals	10-44
10.4.2.1 Alarm Indication Signal	10-44
10.4.2.2 Remote Alarm Indication	10-44
10.4.3 Applications	10-45
10.5 DS2	10-46
10.5.1 DS2 Frame Structure	10-46
10.5.2 Alarm Signals	10-48
10.5.2.1 Alarm Indication Signal	10-48
10.5.2.2 Remote Alarm Indication	10-48
10.5.3 Maintenance	10-49
10.5.4 Applications	10-49
10.6 DS3	10-50
10.6.1 DS3 Frame Structure (M-Frame Format)	10-50
10.6.2 Alarm and Idle Signals	10-51
10.6.2.1 Alarm Indication Signal	10-51
10.6.2.2 Remote Defect Indicator (RDI)	10-51
10.6.2.3 Idle Signal	10-52
10.6.3 M23 Application	10-52
10.6.4 C-Bit Parity Application – 28 DS1 Channels	10-55
10.6.4.1 Application Identification	10-56
10.6.4.2 Far End Alarm and Control Signals	10-57
10.6.4.2.1 Far End Alarm/Status Signals	10-57
10.6.4.2.2 Control Signals	10-58
10.6.4.3 DS3 Path Parity Bits	10-60

- 10.6.4.4 FEBE Function 10-61
- 10.6.4.5 Terminal-to-Terminal Path Maintenance Data Link 10-61
 - 10.6.4.5.1 LAPD Frame Details 10-61
 - 10.6.4.5.2 Information Field Content 10-64
 - 10.6.4.5.3 Special Carrier Usage 10-65
- 10.6.5 Unchannelized DS3 Application 10-65
- 10.7 DS4NA 10-66
 - 10.7.1 Frame Structure 10-66
 - 10.7.2 Alarm Signals 10-69
 - 10.7.2.1 Alarm Indication Signal 10-69
 - 10.7.2.2 Remote Defect Indication 10-69
 - 10.7.3 Maintenance Channels 10-69
 - 10.7.4 Performance Monitoring 10-69
 - 10.7.5 DS4NA Application: M34 Multiplex Format - 3 DS3 Channels 10-69
 - 10.7.5.1 Alarms 10-70
 - 10.7.5.2 Maintenance Channels 10-70

11 Coding Laws

- 11.1 General 11-1
- 11.2 Pulse Code Modulation 11-1
 - 11.2.1 Compression Law 11-2
 - 11.2.2 Coder/Decoder (CODEC) Transfer Characteristics 11-2
 - 11.2.3 Decision Levels 11-5
 - 11.2.4 Code Assignments 11-5
- 11.3 Adaptive Differential Pulse Code Modulation 11-7
 - 11.3.1 General 11-7
 - 11.3.2 ADPCM Coding Algorithm 11-7
 - 11.3.2.1 General 11-7
 - 11.3.2.2 ADPCM Encoder 11-9
 - 11.3.2.3 ADPCM Decoder 11-9
 - 11.3.3 ADPCM Encoder Principles 11-9
 - 11.3.3.1 Input PCM Format Conversion 11-10
 - 11.3.3.2 Difference Signal Computation 11-10
 - 11.3.3.3 Adaptive Quantizer 11-10
 - 11.3.3.4 Inverse Adaptive Quantizer 11-11
 - 11.3.3.5 Quantizer Scale Factor Adaptation 11-11
 - 11.3.3.6 Adaptation Speed Control 11-12
 - 11.3.3.7 Adaptive Predictor and Reconstructed Signal Calculator 11-13
 - 11.3.3.8 Tone and Transition Detector 11-14
 - 11.3.4 ADPCM Decoder Principles 11-15
 - 11.3.4.1 Inverse Adaptive Quantizer 11-15
 - 11.3.4.2 Quantizer Scale Factor Adaptation 11-15
 - 11.3.4.3 Adaptation Speed Control 11-15
 - 11.3.4.4 Adaptive Predictor and Reconstructed Signal Calculator 11-16
 - 11.3.4.5 Tone and Transition Detector 11-16
 - 11.3.4.6 Output PCM Format Conversion 11-16
 - 11.3.4.7 Synchronous Coding Adjustment 11-16
 - 11.3.5 Computational Details 11-17
 - 11.3.6 Digital Test Sequences 11-17

12 Physical Design

12.1 Human Factors Criteria	12-1
12.1.1 Introduction	12-1
12.1.2 Characteristics of the User, NE and Environment – Assumptions	12-2
12.1.2.1 The User	12-2
12.1.2.2 The NE	12-2
12.1.2.3 The Environment	12-2
12.1.3 NE Physical Criteria	12-3
12.1.3.1 General NE Criteria	12-3
12.1.3.1.1 Visual and Audible Interface	12-3
12.1.3.1.1.A General Criteria	12-3
12.1.3.1.1.B Alarm Indicators	12-4
12.1.3.1.1.C Power-On Indicators	12-4
12.1.3.1.1.D Display and Terminal Information	12-5
12.1.3.1.1.E Display Maintenance	12-5
12.1.3.1.2 Manual Controls	12-5
12.1.3.1.2.A Relationship to USI Device Control	12-5
12.1.3.1.2.B Control Layout and Position	12-6
12.1.3.1.2.C Critical and Service-Affecting Controls	12-6
12.1.3.1.2.D Other Types of Controls	12-7
12.1.3.1.3 Labels	12-7
12.1.3.1.3.A General Labeling Criteria	12-7
12.1.3.1.3.B Label Positioning	12-9
12.1.3.1.3.C Labels for Groups of Items	12-9
12.1.3.1.3.D Safety-Related Labels	12-9
12.1.3.1.3.E Electrostatic Discharge (ESD) Labels	12-10
12.1.3.1.3.F Circuit Board and Slot Labels	12-10
12.1.3.1.4 Numbering	12-10
12.1.3.1.4.A Standard Scheme	12-10
12.1.3.1.4.B Alphanumeric Numbering	12-11
12.1.3.1.5 Safety	12-11
12.1.3.1.5.A Movable Components	12-11
12.1.3.1.5.B Sharp Edges and Pinch Points	12-11
12.1.3.1.5.C Protrusions	12-12
12.1.3.1.5.D Electrical Power	12-12
12.1.3.1.5.E Electric Shock or Startle	12-12
12.1.3.1.5.F Hot Surfaces	12-13
12.1.3.1.6 User-System Dialogue	12-13
12.1.3.2 Specific NE Component Criteria	12-13
12.1.3.2.1 Memory Components	12-13
12.1.3.2.1.A Operation	12-13
12.1.3.2.1.B Protection	12-14
12.1.3.2.1.C Offline Memory	12-14
12.1.3.2.2 Circuit Boards	12-15
12.1.3.2.2.A Circuit Board Seating	12-15
12.1.3.2.2.B Circuit Board Faceplates	12-15
12.1.3.2.2.C Circuit Board Latches	12-15
12.1.3.2.2.D Circuit Board Insertion - Removal Force	12-16
12.1.3.2.2.E Circuit Board Power Conditions	12-16
12.1.3.2.2.F Circuit Board Weight	12-16

- 12.1.3.2.2.G Circuit Board Size and Shape 12-16
- 12.1.3.2.2.H Device Protection 12-16
- 12.1.3.2.2.I Common Units 12-17
- 12.1.3.2.2.J Exclusive Control of Parameters 12-17
- 12.1.3.2.3 Bay and Panel Layout and Considerations 12-17
- 12.1.3.3 NE Criteria Related to Specific Operations 12-18
 - 12.1.3.3.1 Installation 12-18
 - 12.1.3.3.2 Provisioning 12-18
- 12.1.3.4 Maintenance 12-18
 - 12.1.3.4.1 Routine Maintenance 12-18
 - 12.1.3.4.2 Alarms 12-19
 - 12.1.3.4.3 Automatic Testing of a Replacement Unit 12-19
 - 12.1.3.4.4 Equipment Failures 12-19
 - 12.1.3.4.5 Power Failures 12-19
 - 12.1.3.4.6 Maintenance Position 12-20
- 12.1.3.5 Circuit and Facility Testing 12-20
- 12.1.3.6 Trouble Isolation 12-20
 - 12.1.3.6.1 Automatic Trouble Isolation and Self-Diagnostics 12-20
 - 12.1.3.6.2 Trouble Indicators 12-21
 - 12.1.3.6.3 Special Test Equipment and Procedures 12-21
 - 12.1.3.6.4 Service Affecting Activity 12-21
 - 12.1.3.6.5 Restoration Of Parameters 12-21
- 12.1.3.7 Software Program Updating 12-21
- 12.1.3.8 Growth of the NE 12-22
- 12.1.3.9 Administration 12-22
- 12.2 Equipment 12-22
- 12.3 NEBS 12-23

13 Power Systems Interfaces

- 13.1 General 13-1
- 13.2 Shared DC Power 13-2
 - 13.2.1 Voltage Limits 13-2
 - 13.2.2 Electrical Noise 13-3
 - 13.2.3 DC Distribution 13-4
 - 13.2.4 Current Drains 13-4
- 13.3 AC Power Interfaces 13-5

14 Electrical Environment and Safety

- 14.1 System-Level ESD and Electrical Fast Transient (EFT) 14-1
- 14.2 Electromagnetic Interference (EMI) 14-1
- 14.3 Lightning and AC Power Fault 14-1
- 14.4 Steady-State Power Induction 14-1
- 14.5 DC Potential Difference 14-1
- 14.6 Electrical Safety 14-2
- 14.7 Corrosion 14-2
- 14.8 Bonding and Grounding 14-2

15 Operations Technology

16 Supplier Documentation

17 Supplier-Provided Training

18 DSn Alarm Surveillance

18.1 Introduction 18-1
18.2 Directly Detected Defects 18-2
 18.2.1 DSn LOS 18-2
 18.2.2 DSn Out of Frame (OOF) 18-3
 18.2.2.1 DSn OOF Defect Detection 18-3
 18.2.2.2 DSn OOF Defect Termination 18-5
18.3 DSn AIS 18-6
 18.3.1 AIS Insertion and Removal 18-6
 18.3.2 AIS Defect Detection 18-9
18.4 DSn Transport Modes 18-10
18.5 DSn Failure Declaration and Clearing 18-11

Appendix A: Deleted Requirement-Objects List

A.1 Requirement Objects Deleted or Not Used as of Issue 2 A-1
A.2 Requirement Objects Deleted as of Issue 3 A-2
A.3 Requirement Objects Deleted as of Issue 4 A-3

References

Acronyms, Abbreviations and Units

Requirement-Object Index

List of Figures

Figure 2-1	HRC for Interoffice DS _n Transport System Availability Objectives	2-4
Figure 2-2	Interoffice Transport System Availability Objectives – DSX-1 to DSX-1	2-4
Figure 2-3	Interoffice Transport System Availability Objectives – DSX-3 to DSX-3	2-5
Figure 2-4	SONET HRC Linear Network Architecture	2-9
Figure 2-5	Downtime Allocations for the 250-Mile HRC	2-11
Figure 2-6	Downtime Allocations for the 50-Mile HRC	2-13
Figure 2-7	Metallic Loop Reference Circuit	2-16
Figure 2-8	Fiber Optic Loop Reference Circuit	2-17
Figure 2-9	Distribution Feeder Outage Objectives Per DS1 Channel	2-19
Figure 5-1	Maximum Detection Times	5-6
Figure 7-1	Input Jitter Tolerance – Category I and II Interfaces	7-6
Figure 7-2	Additional Input Jitter Tolerance - Category II Interfaces	7-7
Figure 7-3	Category II Interface to Category I Interface Jitter Transfer	7-11
Figure 7-4	Category I Interface to Category I Interface Jitter Transfer	7-12
Figure 7-5	Category II Interface to Category II Interface Jitter Transfer	7-13
Figure 9-1	Example of CMI Coding	9-5
Figure 9-2	8-Position Keyed Jack	9-6
Figure 9-3	50-Position Keyed Jack	9-7
Figure 9-4	Synchronous Digital Data Loop Transmission	9-11
Figure 9-5	DS1 Interface Isolated Pulse Mask and Corner Points	9-20
Figure 9-6	DS1C Interface Isolated Pulse Mask and Corner Points	9-23
Figure 9-7	DS2 Interface Isolated Pulse Mask and Equations	9-26
Figure 9-8	DS3 Interface Isolated Pulse Mask and Equations	9-29
Figure 9-9	DS4NA Interface Eye Diagram	9-32
Figure 9-10	DS4NA Maximum Equipment Output Eye Diagram	9-33
Figure 9-11	DS1A Interface Isolated Pulse Mask and Corner Points	9-37
Figure 10-1	Scheduled Performance Report Message Format	10-32
Figure 10-2	ESF DL Performance Report Message Example	10-33
Figure 10-3	DS1C Frame Format	10-44
Figure 10-4	DS2 Frame Structure	10-47
Figure 10-5	DS2 Frame Overhead Structure	10-48
Figure 10-6	DS3 Signal Format	10-51
Figure 10-7	M23 Application – Seven DS2 Channels	10-54
Figure 10-8	Q.921 (LAPD) Message Structure	10-63
Figure 10-9	DS4NA Frame Structure	10-67
Figure 10-10	DS4NA Application: M34 Multiplex Format-Three DS3 Channels	10-71
Figure 11-1	CODEC Transfer Characteristic – Information Frame	11-3
Figure 11-2	CODEC Transfer Characteristic – Signaling Frame	11-4
Figure 11-3	Simplified Block Diagrams	11-8
Figure 11-4	Encoder Block Schematic	11-10
Figure 11-5	Decoder Block Schematic	11-15

List of Tables

Table 2-1	DS3 Outage Allocation – 79 Minutes	2-7
Table 2-2	DS1 Outage Allocation – 105 Minutes	2-8
Table 2-3	50- and 250-Mile HRC Characteristics	2-12
Table 6-1	Maximum Recovery Times – Phase Hits	6-1
Table 6-2	Radio System Recovery Times – Temporary Signal Interruptions	6-2
Table 7-1	Maximum Permissible Timing Jitter at DS _n Network Interfaces	7-3
Table 9-1	Examples of B8ZS Coding Used at the DS1 and DS1C Rates	9-2
Table 9-2	Examples of B6ZS Coding Used at the DS2 Rate	9-3
Table 9-3	Pin Assignments for 8-Position Series Jack	9-6
Table 9-4	Frequency Constraints	9-9
Table 9-5	Line Rates at the NI	9-12
Table 9-6	Pulse Amplitudes of Ideal Pulses Used to Define Template Limits	9-14
Table 9-7	Loss Limits and Nyquist Frequencies	9-16
Table 9-8	DS1 Interface Specification	9-18
Table 9-9	DS1C Interface Specification	9-22
Table 9-10	DS2 Interface Specification	9-25
Table 9-11	DS3 Interface Specification	9-28
Table 9-12	DS4NA Interface Specification	9-31
Table 9-13	DS1A Interface Specification	9-36
Table 10-1	Secondary Channel Bit Rates	10-5
Table 10-2	Truth Table for {SC XNOR C ₂ }	10-8
Table 10-3	Framing Patterns	10-8
Table 10-4	Maintenance and Failure Signals	10-9
Table 10-5	DS0 Byte Frame Formats	10-12
Table 10-6	Repetition Rates	10-12
Table 10-7	DS0-A Frame Format for the 19.2-kb/s Rate (No Error Correction)	10-13
Table 10-8	DS0-B Frame Format for 2.4, 4.8, 9.6 kb/s	10-14
Table 10-9	DS0-B Framing Patterns	10-14
Table 10-10	DS0-B Byte Format for the 19.2-kb/s Rate	10-15
Table 10-11	Error Correction DS0-A Format for 19.2 kb/s	10-16
Table 10-12	Synchronous Digital Data Control Codes	10-19
Table 10-13	LSC and MAP Codes for Latching Loopbacks	10-22
Table 10-14	Superframe Format	10-25
Table 10-15	Extended Superframe Format	10-27
Table 10-16	ESF Data Link Unscheduled Messages	10-37
Table 10-17	C-Bit Parity – C-Bit Functions and Values	10-56
Table 10-18	Assigned Alarm and Status FEAC Codewords	10-58
Table 10-19	Assigned Loopback Control Codewords	10-59
Table 10-20	Unassigned Codewords	10-60
Table 10-21	Path, Idle Signal, and Test Signal Identification – Message Structure	10-65
Table 10-22	DS4NA Frame Overhead Structure	10-68
Table 11-1	Code Decision Levels	11-5
Table 11-2	Assignment of Transmitted Codes and Decoded Level	11-6
Table 11-3	Definition of W-bits in Table 11-2	11-6

Table 11-4	Quantizer Normalized Input/Output Characteristic	11-11
Table 13-1	Voltage Range for Nominal Voltage of -48 V	13-2
Table 18-1	LOS Defect Termination Limits	18-3
Table 18-2	DSn OOF Defect Detection	18-4
Table 18-3	DSn OOF Defect Termination	18-6
Table 18-4	DSn AIS Insertion Times	18-7
Table 18-5	DSn AIS Removal Times	18-9
Table 18-6	DSn AIS Defect Detection and Termination	18-10
Table 18-7	Hierarchy of Near-End Failures	18-12